



SMC-02-1091

December 15, 2003

To: Commissioner for Patents
P.O.Box 1450
Alexandria, VA 22313-1450

Fr: George O. Saile, Reg. No. 19,572
28 Davis Avenue
Poughkeepsie, N.Y. 12603

Subject: | Serial No. 10/669,515 09/24/03 |

Wen-Tai Wang et al.

DYNAMICALLY ADJUSTABLE DECOUPLING
CAPACITANCE TO REDUCE GATE LEAKAGE
CURRENT

INFORMATION DISCLOSURE STATEMENT

Enclosed is Form PTO-1449, Information Disclosure Citation
In An Application.

The following Patents and/or Publications are submitted to
comply with the duty of disclosure under CFR 1.97-1.99 and
37 CFR 1.56.

CERTIFICATE OF MAILING

I hereby certify that this correspondence is being
deposited with the United States Postal Service as first class
mail in an envelope addressed to: Commissioner for Patents,
P.O. Box 1450, Alexandria, VA 22313-1450, on December 19, 2003.

Stephen B. Ackerman, Reg.# 37761

Signature/Date

The following two U.S. Patents teach a circuit to detect a defective decoupling capacitor during a power-up test:

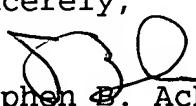
- 1) U.S. Patent 5,506,457 to Krauter et al., "Electronic Switch for Decoupling Capacitor."
- 2) U.S. Patent 6,307,250 to Krauter et al., "Electronic Switch for Decoupling Capacitor."

U.S. Patent 5,789,964 to Voldman, "Decoupling Capacitor Network for Off-State Operation," discloses a method to detect a defective decoupling capacitor during power-up and to switch in a capacitor during an ESD event.

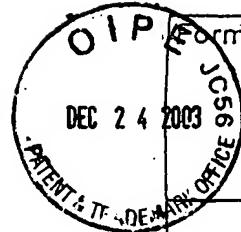
U.S. Patent Application Publication US 2002/0081832 A1 to Bernstein et al., "Intralevel Decoupling Capacitor, Method of Manufacture and Testing Circuit of the Same," describes a circuit to test decoupling capacitors in an integrated circuit device.

In the article, "Interconnect and Circuit Modeling Techniques for Full-Chip Power Supply Noise Analysis," by Chen et al., in IEEE Transactions on Components, Packaging, and Manufacturing Technology - Part B, Vol. 21, No. 3, Aug. 1998, pp. 209-215, a capacitor and switch combination is described.

Sincerely,



Stephen B. Ackerman, Reg.# 37761



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Form PTO-1449

INFORMATION DISCLOSURE CITATION
IN AN APPLICATION

(Use several sheets if necessary)

Doctor Munroe (Captain)

TSMC-02-1091

Afternoon Hours

10/669,515

Appleton

Wen-Tai Wang et al.

Filing Date

09/24/03

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U. S. PATENT DOCUMENTS

FOREIGN PATENT DOCUMENTS

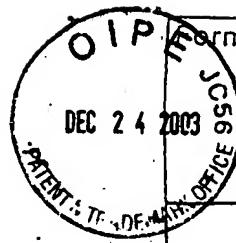
| | DOCUMENT NUMBER | DATE | COUNTRY | CLASS | SUBCLASS | TRANSLATION | |
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OTHER DOCUMENTS (Including Author, Title, Date, Portion or Pages, Etc.)

Article "Interconnect and Circuit Modeling Techniques for Full-Chip Power Supply Noise Analysis," by Chen et al., in IEEE Trans. on Components, Packaging, and Manuf. Tech. - Part C, Vol. 21, No. 3, Aug. 1998, pp. 209-215.

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| EXAMINER | DATE CONSIDERED |
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EXAMINER: Initial if citation considered, whether or not citation is in conformance with MPEP § 609; Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to the applicant.



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INFORMATION DISCLOSURE CITATION IN AN APPLICATION

(Use several sheets if necessary)

Doctor Number (Optional)

Appetizer Number

TSMC-02-1091

10/669,515

Applicant

Wen-Tai Wang et al.

Ending Date

09/24/03

U. S. PATENT DOCUMENTS

FOREIGN PATENT DOCUMENTS

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OTHER DOCUMENTS (Including Author, Title, Date, Portion or Pages, Etc.)

U.S. Patent App. Publication US 2002/0081832 A1 to
Bernstein et al., Pub. June 27, 2002, "Intralevel
Decoupling Capacitor, Method of Manufacture and
Testing Circuit of the Same".

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